DESIGN OF RING OSCILLATOR USING CS-CMOS FOR MIXED SIGNAL SOCs

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ABSTRACT

This paper reports design of a ring oscillator using CS-COMS low noise logic family for mixed signal SOCs. Design has been implemented using 180nm technology with 1.8V supply voltage using CS- CMOS logic. CS-CMOS logic efficiently reduce switching noise while maintaining the speed as compare to the other logics like CSL, CBL etc.

After completion of the design authors have simulated the design in Spectre simulator and obtained the best simulation results. Authors have determined the parameters like phase noise, delay.

KEYWORDS: Cadence, Current Balanced Logic (CBL), Current Steering CMOS (CS-CMOS), Current Steering Logic (CSL), Mixed Signal SOCs, Ring Oscillator, Spectre Simulator